



Analog Mixed-Signal Verification

DVClub, Monday 6th December 2010 from 11.30 to 14.00

At various locations

- **Bristol:** Infineon, Great Western Court, Hunts Ground Road, Stoke Gifford, BS34 8HP
- **Cambridge:** The ARM office in Cambridge (110 Fulbourn Road, Cambridge, CB1 9NJ, England)
- **Remote Access:** Access from your desktop (details to follow)
- **Eindhoven:** Details to follow

All times below are UK times

11.30	Networking, drinks and buffet
12.00	Introduction, Mike Bartley, TVS
12.05	“Advanced methodologies used for top-level verification of mixed signal products”, Roger Witlox, Sr. Verification Engineer, PL Integrated IVN & FlexRay, NXP The described verification approach is used to verify IC’s that are used in automotive in-vehicle networks. Examples are LIN, CAN and Flexray transceivers. Transceivers are mixed signal designs that translate a digital signal into an analog signal and vice versa and are used in the physical layer of a network. Due to trends like power modes, digital trimming, auto calibration and integration these mixed signal designs are becoming more and more complex. As a result a commonly used architecture contains a central digital state-machine that controls the surrounding analog modules. This all requires a more advanced overall verification approach. One of the instruments used in this overall verification approach is top-level (chip-level) verification. The goal of top-level verification is to prove interconnect and interoperability. It assumes that functionality is verified at IP-level. The types of bugs hunted with this approach include: wrong polarity, flipped busses and chicken & egg problems. Top-level is always subject to late design changes and often timing critical towards tape-out, therefore the following methods are used: Self-checking, Modeling, Reusability and Functional coverage.
12.40	“Analogue Behavioural Modelling: An Inconvenient Truth”, Dave Wiltshire, Texas Instruments, UK The complexity of SERDES designs has resulted over several years in increased analogue complexity. This extra complexity means that simple behavioural models cannot be used to test everything in a design. This presentation will discuss the different strategies that have been developed with the TI SERDES design team solve the problem of verifying a complex mixed signal design using Verilog simulators. The following development strategies will be used. Using standard digital verilog simulation: <ul style="list-style-type: none">▪ Model analogue behaviour using verilog reals▪ Solving how to pass verilog reals across module boundaries Migrating to VerilogA behavioural models <ul style="list-style-type: none">▪ Verifying that the models match the transistor implementation▪ Solving the simulation speed issues (wreal)
13.15	“Using assertions in AMS verification”, Scott Little, AMS Verification Engineer, Freescale Assertions have been used successfully in digital verification methodologies for a number of years. As the size and complexity of AMS blocks and SoC designs increase, there is an increasing need for assertions capable of specifying and checking AMS behaviors. We discuss ongoing work within Freescale and the Accellera AMS Assertions sub-committee to develop, standardize, and deploy AMS assertions.
13.50	Networking, drinks and buffet
14.00	Finish

Don't miss out – register now for this **free** event at <http://dvclubbristoldec2010.eventbrite.com/>

or get more details by emailing Mike Bartley (mike@tandvsolns.co.uk).

This event is sponsored by ARM, Infineon, the NMI and TVS

