

asureVIP™ from TVS

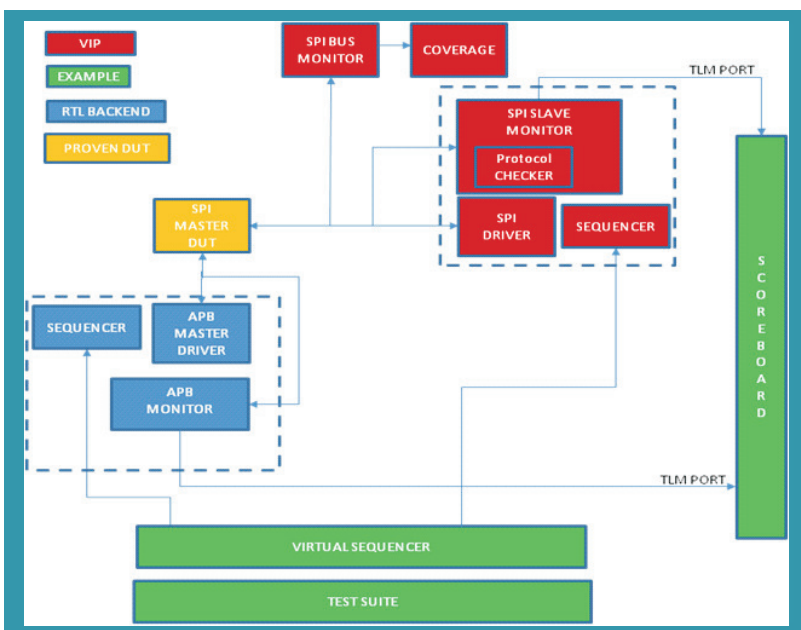
TVS SPI OVM SLAVE VIP

OVERVIEW

Test and Verification Solutions offers an SPI OVM Slave VIP as part of its asureVIP™ series of offerings. This is a highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment. The Slave VIP was used in successfully verifying a DUT Master, later silicon proven.

The VIP comes with a Bus Monitor for performing all protocol checks. The monitor also performs key protocol checks and reports errors for non compliance with Freescale SPI block guide.

BLOCK DIAGRAM



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FEATURES

- Supports Slave mode
- Supports Bi-directional mode
- Double-buffered operation
- Control of SPI operation during wait mode
- Multiple baud rate support



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TECHNICAL SPECIFICATION

Part Number	asureVIP_SPI_S
Description	SPI OVM SV based Slave VIP
Provider	Test and Verification Solutions
Languages Supported	System Verilog
Methodology	OVM 2.1.1
Simulators	Cadence Incisive, Mentor Questa
Compliance	SPI Freescale Block Guide v4.01
Availability	August 2011

ABOUT US

TVS delivers an independent verification service that not only reduces your costs and time-to-market, but also improves product quality.

TVS combines skills and experience in software testing, hardware verification and outsourcing to provide customers with an efficient, well-managed, quality assurance service.

TVS provides both consultancy and execution services using experienced engineering resources in several locations around the world. TVS removes the pain and risk from outsourcing leaving you with just the benefits.

To learn more about our offerings, write to us at vip@tandvsolns.co.uk

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BENEFITS

- Highly Flexible, Independent and Configurable SPI Slave VIP
- Proven against Silicon Proven DUT
- Less TAT in integrating into SOC Verification environments

DELIVERABLES

- VIP user Guide
- SPI Slave OVM VIP
- Sample Testbench Integrated with proven SPI Master DUT / APB Master Driver/Monitor
- Sample Scoreboard
- Sample Virtual Sequencer



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